

Patent claims

1. An organic logic gate comprising at least one charging field effect transistor (charging FET) and at least one switching field effect transistor (switching FET), the charging FET having at least one gate electrode, a source electrode and a drain electrode, characterized in that the gate electrode of the charging FET is potential-free.
2. The organic logic gate as claimed in claim 1, characterized in that the gate electrode of the charging FET is capacitively coupled to the source electrode of the charging FET.
3. The organic logic gate as claimed in claim 2, characterized in that the capacitive coupling is achieved by means of the gate electrode overlapping the source electrode of the charging FET.
4. The organic logic gate as claimed in one of the preceding claims, characterized in that the gate electrode of the charging FET is resistively coupled to the source electrode of the charging FET.
5. The organic logic gate as claimed in one of the preceding claims, characterized in that the gate electrode of the charging FET is capacitively coupled to the drain electrode of the charging FET.
6. The organic logic gate as claimed in claim 5, characterized in that the capacitive coupling is achieved by means of the drain electrode overlapping the gate electrode of the charging FET.
7. The organic logic gate as claimed in one of the preceding claims, characterized in that the gate electrode of the charging FET is resistively coupled to the drain electrode of the charging FET.

8. The organic logic gate as claimed in one of the preceding claims, characterized in that the organic logic gate is constructed without plated-through holes.